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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,975	09/26/2003	Robin Alexis Takasugi	10014268-1	3620

22879 7590 02/06/2006

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EXAMINER

TSAI, SHENG JEN

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/672,975		TAKASUGI ET AL.	
	Examiner		Art Unit	
	Sheng-Jen Tsai		2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 December 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Amendment filed on December 19, 2005 regarding application 10,672,975 filed on September 26, 2003.

2. Claims 1, 9-10 and 20 have been amended.

Claims 1-25 are pending in the application under consideration.

3. ***Response to Amendments and Remarks***

Applicant's amendments and remarks have been fully and carefully considered.

In response, another round of claim analysis based on the previously relied on reference (Kaneko et al., US 6,427,184), in combination with a previously cited but not relied on prior art (Bates, Jr. et al., US 6,253,289), has been embarked. Refer to the corresponding sections of the claim analysis for details.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko et al. (US 6,427,184), and in view of Bates, Jr. et al. (US 6,253,289).

As to claim 1, Kaneko et al. disclose a **prefetch controller** [Disk Drive with Prefetch and Writeback Algorithm for Sequential and Nearly Sequential Input/Output Streams (title); the magnetic disk processor, figure 1, 1] **for controlling retrieval of data from a data storage device** [magnetic disk devices (abstract); figure 1, 9A~9C]

in response to a current host command received from a host device [Host, figure 1, 2], the prefetch controller comprising:

a sequential read detector [the I/O stream monitor, figure 1, 11] configured to generate a new sequential read indication for the current host command if the current host command and a previously received host command specify read operations that are non-sequential [figure 3; figure 6; column 1, lines 23-33; column 2, lines 11-26; column 5, lines 15-67]; and

a transfer length generator configured to provide a first transfer length value [the first transfer length has an I/O stream size = I/O stream size + “size” (column 3, lines 10-31; column 5, lines 45)] to the data storage device if the new sequential read indication is generated for the current host command [column 3, lines 10-31; column 5, lines 45], and provide a second transfer length value [the second transfer length has an I/O stream size = “size” (column 3, lines 10-31; column 5, lines 45)] to the data storage device if the new sequential read indication is not generated for the current host command [column 3, lines 10-31; column 5, lines 45]; and

wherein the first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host command [see below].

With respect to claim 1, Kaneko et al. only implicitly refer to the limitation of **“wherein the first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host command”** [the corresponding “prefetch value” is the “prefetch size” as shown in figure 2 associated with each of the I/O stream requests, noted that the parameter “prefetch size” is

independent, and in addition to, the parameter "I/O stream size;" the flowchart in figure 3 shows that, when it is a sequential I/O stream (YES on step S103), the I/O stream size will be updated (step S105) by calling the prefetch activator (step S108), which calculates a prefetch start address from "stream start address" and "prefetch size" to newly activate a prefetch (column 5, lines 61-65; column 7, lines 7-20)].

Further, Bates, Jr. et al. explicitly teach in their invention "Maximizing Sequential Read Streams While Minimizing the Impact on Cache and Other Applications" a method and apparatus of maximizing sequential read streams in a data storage device [abstract] in which the prefetch size (i.e., the data transfer length) equals the sum of a previous prefetch size and a read request size [figure 3, step 64].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the common and widely adopted practice of using adding a prefetch value to a requested data-read size to determine the starting address as well as the total data transfer size, as demonstrated by Bates, Jr. et al. explicitly and by Kaneko et al. implicitly, and the lack of patentable significance of this limitation.

As to claim 2, Kaneko et al. teach that **the first transfer length value** [the first transfer length has an (I/O stream size) = (I/O stream size) + "size" (column 5, lines 45)] **is larger than the second transfer length value** [the second transfer length has an (I/O stream size) = "size" (column 5, line 33); and (I/O stream size) + "size" is greater than "size"]. Also refer to "As to claim 1."

As to claim 3, Kaneko et al. teach that **the sequential read detector**

comprises:

operation compare logic configured to compare an operation specified in the current host command to an operation specified in the previously received host command, and generate a first indication for the current host command if the compared operations are both read operations [figure 3, S106 indicates if both are READ commands; column 5, lines 51-61].

As to claim 4, Kaneko et al. teach that **the sequential read detector further comprises:**

address compare logic configured to compare a first address associated with the current host command to a second address associated with the previously received host command, and generate a second indication for the current host command if the compared addresses are indicative of sequential operations [figure 3, S107 indicates if the difference of the addresses is greater or smaller than a threshold; column 2, lines 18-26; column 2, lines 66-67; column 3, lines 1-9].

As to claim 5, Kaneko et al. teach that **the sequential read detector further comprises: a sequential read indication generator configured to generate the new sequential read indication if the first and the second indications are not generated for the current host command** [figure 3; column 5, lines 15-67].

As to claim 6, Kaneko et al. teach that **the sequential read detector comprises: a plurality of registers** [figure 2 shows a plurality of entries, with each entry having a plurality of registers] **for storing an opcode specified in the current host command** [R/W type of entry 2], **an opcode specified in the previous host command** [R/W

type of entry 1], a **start address associated with the current host command** [stream start address of entry 2], and an **end address associated with the previous host command** [stream start address of entry 1].

As to claim 7, Kaneko et al. teach that **the sequential read detector further comprises:**

opcode compare logic for comparing the stored opcodes [R/W type, figure 2];
address increment logic for incrementing the stored end address, thereby generating an incremented end address [last address + 1, column 2, lines 17-26];
and
address compare logic for comparing the stored start address and the incremented end address [figure 3, S107].

As to claim 8, Kaneko et al. teach that **the sequential read detector further comprises:**
a sequential read indication generator configured to generate the new sequential read indication based on outputs of the opcode compare logic and the address compare logic [figure 3; column 2, lines 17-26; column 5, lines 15-67].

As to claim 9, Kaneko et al. teach that **the transfer length generator comprises:**
a first register for storing the prefetch value [prefetch size, figure 2; update prefetch size, figure 4];
a second register for storing a zero value [this corresponds to no prefetch]; **and**

a multiplexer coupled to the first and the second registers, the multiplexer responsive to the new sequential read indication for selectively outputting the prefetch value or the zero value [the corresponding multiplexer is the decision/selection of S103, figure 3, which indicates if there is a new sequential read, if a new sequential read is detected, S104 is executed without prefetch, essentially selecting a zero value for the prefetch size (figure 3; column 5, lines 15-67)].

As to claim 10, Kaneko et al. teach that **the transfer length generator further comprises:**

a third register for storing the transfer length value specified in the current host command [the I/O stream size (figure 2; figure 3, S105; column 2, lines 27-44; column 3, lines 10-31)].

As to claim 11, Kaneko et al. teach that **the transfer length generator further comprises:**

an adder for adding the value stored in the third register and the value output by the multiplexer [(I/O stream size) = (I/O stream size) + "size" (column 5, lines 45)].

As to claim 12, Kaneko et al. disclose **a method of transferring data between a host electronic device** [figure 1, 2] **and a data storage device** [figure 1, 3], **the method comprising:**

receiving a current read command [figure 2] **from the host electronic device, the current read command specifying a first transfer length value** [I/O stream size, figure 2];

identifying whether the current read command is non-sequential to a previously received read command [figure 3; column 2, lines 17-26];
adding a prefetch length value [prefetch size] to the first transfer length value if the current read command and the previous read command are non-sequential, thereby generating a second transfer length value $[(I/O \text{ stream size}) = (I/O \text{ stream size}) + \text{"size"}]$ (column 5, lines 45).; and
outputting the second transfer length value to the data storage device [figure 1].

Regarding claims 13-14, Bates, Jr. et al. teach buffering the data received from the storage device and outputting the buffered data to the host [a cache (figure 1, 24) is used as a buffer for data destined to the host (column 2, lines 40-49)].

As to claim 15, refer to "As to claim 3" and "As to claim 4."

As to claim 16, refer to "As to claim 9" and "As to claim 11."

As to claim 17, Kaneko et al. disclose a **memory device** [figure 1, 3]

comprising:

storage means for storing data [figure 1, 9A~9C];

host [figure 1, 2] interface means for receiving host commands from a host

electronic device [figure 1, 1];

sequential read detection means for identifying whether a current host command specifies a non-sequential read operation [refer to "As to claim 1"]; and

transfer length generation means for adding a prefetch length value to a transfer length value specified in the current host command if the current host command specifies a non-sequential read operation, the transfer length generation means

configured to output a sum of the prefetch length value and the transfer length value to the storage means [refer to "As to claim 1" and "As to claim 12"].

As to claim 18, refer to "As to claim 15."

As to claim 19, refer to "As to claim 9" and "As to claim 11."

As to claim 20, refer to "As to claim 1," "As to claim 12," and "As to claim 17."

As to claim 21, refer to "As to claim 2."

As to claim 22, refer to "As to claim 3."

As to claim 23, refer to "As to claim 4."

As to claim 24, refer to "As to claim 5."

As to claim 25, Kaneko et al. teach that **the computer-readable medium of claim 20, wherein the method further comprises:**
storing an opcode specified in the current host command, an opcode specified in the previous host command, a start address associated with the current host command, and an end address associated with the previous host command
[figure 2].

As to claim 26, refer to "As to claim 9" and "As to claim 11." Also, column 2, lines 17-26.

As to claim 27, refer to "As to claim 9" and "As to claim 11."

As to claim 28, refer to "As to claim 9."

As to claim 29, refer to "As to claim 10."

As to claim 30, refer to "As to claim 11."

6. Related Prior Art

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Greiner et al., (US 6,216,208), "Prefetch Queue Responsive to Read Request Sequences."
- Kanai et al., (US 6,341,335), "Information Processing System for Read Ahead Buffer memory Equipped with Register and Memory Controller."
- Hicken et al., (US 6,092,149), "Disk Drive cache System Using a Dynamic Priority Sequential Stream of Data Segments Continuously Adapted According to Prefetched Sequential Random, and Repeating types of Accesses."
- Desai et al., (US 6,789,171), "Computer System Implementing a Multi-threaded Stride Prediction Read Ahead Algorithm."
- Yu et al., (US 6,606,717), "Cache Control method and System for Mixed Streaming and Non-Streaming data."
- Henry et al., (US 6,917,990), "Method and Structure for Read Prefetch in a Storage Complex Architecture."

Conclusion

7. Claims 1-30 are rejected as explained above.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

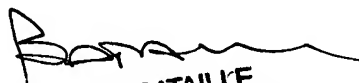
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

February 1, 2006


PIERRE BATAILLE
PRIMARY EXAMINER
2/1/06